Education

- **Southeast University**, Wuxi, China
  - M.Eng. in Integrated Circuit Engineering, 2026–2029 (expected)
- **Wuhan University of Technology**, Wuhan, China
  - B.Eng. in Integrated Circuit Design and Integrated Systems, 2022–2026

Research Interests

- DFT for advanced packaging
- Chip security and reliability
- EDA and optimization for 2.5D/3D integrated systems
- Multi-physics-aware planning

Selected Projects

FPGA-Based Design for Testability

Designed scan chains, LFSR/MISR-based BIST, and fault injection in Verilog; verified on FPGA. Outstanding thesis.

Automated IC Testing on ATE

End-to-end workflow from datasheet analysis to test-vector generation. **National Second Prize**, 9th National IC Competition.

Honors

- **National Scholarship**, Ministry of Education of China
- **National Second Prize**, 9th National College Student IC Innovation and Entrepreneurship Competition, 2025
- **National Third Prize**, 15th National Mathematics Competition for College Students, 2024
- **National Third Prize**, 12th "Da Tang Cup" National College Student New-Generation Information and Communication Technology Competition, 2025
- **Outstanding Student**, Wuhan University of Technology, three times
- **Outstanding Volunteer**, Jingzhou, China

Skills

- **Languages:** C/C++, Python, Verilog/SystemVerilog, Tcl
- **Tools:** VCS, Verdi, Design Compiler, Modelism, Linux, PrimeTime

Last updated: August 2026.